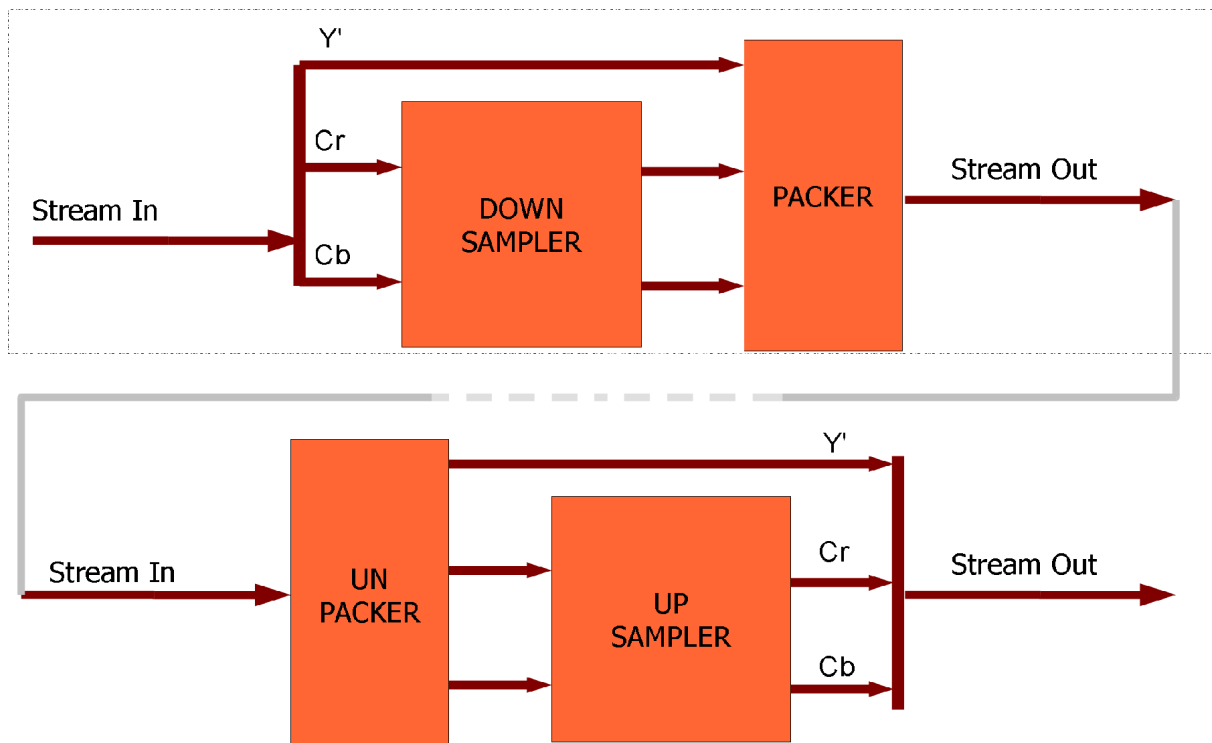


Chrominance Re-sampling Unit

Product Outline

A couple of IP blocks that provide up and down sampling of chroma pixel values

The DIAPLOUS Color Re-sampler blocks provide fully configurable conversion from/to a stream of Y'CrCb 4:4:4 pixels to/from a stream of pixels with the Chroma values sub-sampled (Y'CrCb 4:x:x).



4:4:4 Pixel Streams: The Down Sampler unit expects a stream of pixels formatted as 24bit Y'CrCb. The stream can be synchronized to "frame valid" and "data valid" inputs. An equivalent stream is generated at the output of the Up Sampler unit (including "frame valid" and "data valid" signals).

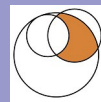
Sub-sampled Pixel Streams: The output of the Packer and the input to the un-Packer units is a stream of pixels with the luma and chroma values arranged according to the selected sub-sampling scheme and the corresponding packing method. The same synchronization signals ("data_valid" and "frame valid") apply; depending on the packing method additional "chroma valid" signals may be required on the stream.

Down Sampler: The down-sampler receives the chroma values of the 4:4:4 stream and generates new chroma pixels depending on the chosen sub-sampling method (see figure in the next page). Appropriate "chroma valid" signals are also generated to facilitate packing of values in a single pixel stream.

Up Sampler: The up-sampler receives chroma values and generates new Y'-synchronous Cr and Cb for integration in a full 4:4:4 pixel stream.

Packer/Un-Packer: The packer unit re-synchronizes the Y' values with the corresponding sub-sampled Cr and Cb. A choice of packing methods is offered. The un-packer performs the reverse operation.

Core Configuration: The code can be configured for various pixel sizes.



Features:

- Two-way Color conversion between YUV444 and sub-sampled chroma formats
- Performs both Re-sampling and Packing
- Easy integration in various pixel flow architectures.

Target Applications:

- Image sensor interfacing
- Display drivers

Size: 500 LEs, 300 FFs (Altera Cyclone III) *

Speed: Pixel Clock 175MHz.

Interfaces:

- YUV444 Pixel-flow Input/Output
- Status/Control Registers
- YUV4:x:x Output/Input

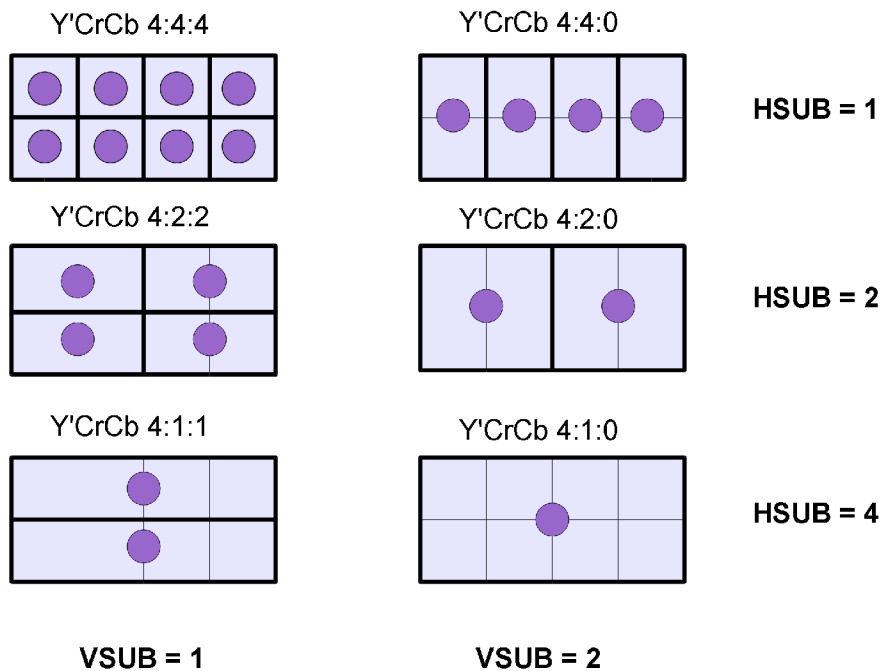
Status:

Working FPGA Implementation.

Demonstration:

Development board including:

- FPGA with RISC Core, Ethernet 10/100 MAC, Sensor Interface, I2C, Memory Interface
- Memories (SDRAM & Flash)
- Ethernet Phy & Connector
- 3Mpixel Color Image Sensor



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* Numbers are preliminary and subject to change