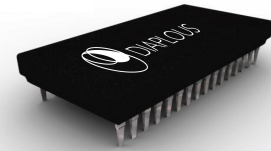


# DIAPLOUS

COMPONENTS FOR VISUAL PERCEPTION

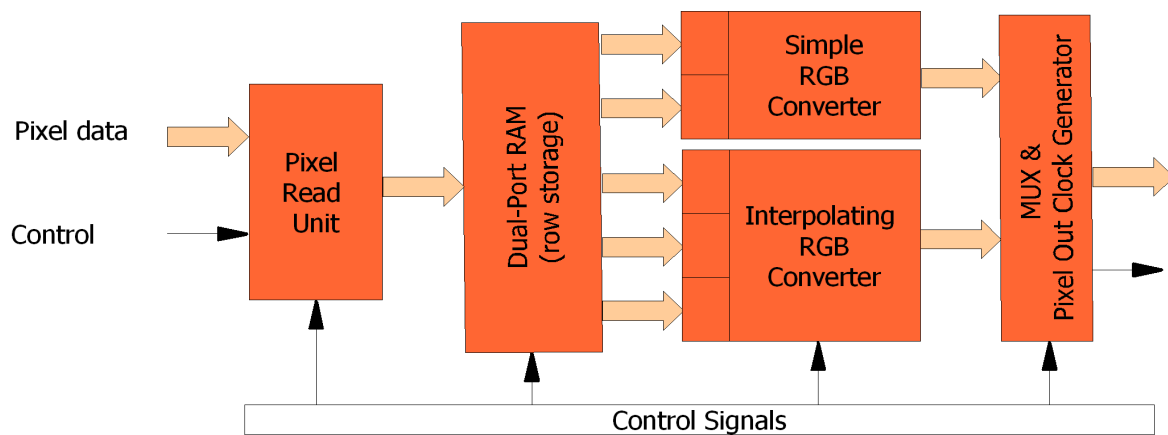


## Bayer to RGB Converter

## Product Outline

### A configurable IP block that converts from parallel Bayer-pattern pixel flow to RGB

The DIAPLOUS Bayer to RGB converter is a flexible unit that can accept a flow of pixel data in Bayer format and generate the corresponding RGB pixels. Two options for conversion are offered: *Simple* (where conversion yields one pixel for each 4 input pixels) and *Interpolation-based* (where a 3x3 set of pixels is used as interpolation input).



**Pixel Read Unit:** This unit feeds the pixels directly in the dual port RAM. It expects the pixels to be available as a synchronous flow or coming from a FIFO. In the later case the unit reads the FIFO to generate this flow.

**Row Storage RAM:** A dual port memory stores multiple rows of pixels as required. At least two rows (the previous and the current one) are needed if simple demosaicing is chosen. In the case of interpolation a number of rows corresponding to the interpolation window is needed. For 3x3 interpolation, 4 rows are required (3 previous, one current).

**Simple RGB Converter:** The simple converter uses only the 4 pixels of an RGGG quad to generate the output. Depending on the required resolution, two methods can apply:

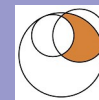
**4to4 demosaicing** (see figure 1). In this case, each pixel is taking its missing color components by simply copying adjacent pixel values. This approach maintains original resolution but is prone to artifact generation.

**4to1 demosaicing** (see figure 2). In this case, each quad generates a single pixel. This approach is more robust in color quality but generates an output image with half the resolution in each direction.

**Interpolating RGB Converter:** The interpolating converter (figure 3) uses a region of 3X3 Bayer pixels around each pixel that needs to be generated. Applying interpolation for the corresponding neighbors to each color components it yields an output image with the same resolution as the original.

**MUX and Pixel-out Clock Generator:** The multiplexer selects demosaicing algorithm. It can also generate a slower pixel clock for the case of *4to1 demosaicing* where the output resolution is reduced.

**Control Signals:** This is the system interface to the block. It contains a number of directly accessible read and write ports which can be mapped as a register file to the host processor.



## Features:

- Configurable Resolution (Up to 32K columns and practically unlimited rows depending on available on-chip memory)
- Read Bayer pattern in Parallel 8 or 10 bits per color component.
- Supports demosaicing to RGB, Monochrome
- Simple and Interpolated Approaches Used
- Enable/Disable Capability

## Target Applications:

- Image sensor interfacing
- Display drivers

**Size:** 1200 Slices, 4 Block RAMs (Xilinx Spartan XC3S1000-5) for images with 2K columns per row.

**Speed:** Pixel Clock 150MHz.

## Interfaces:

- Pixel-flow Input
- Status/Control Registers
- Pixel-flow Output

## Software:

- C Header File with Register Definitions

## Status:

Working FPGA Implementation.

## Demonstration:

Development board including:

- FPGA with RISC Core, Ethernet 10/100 MAC, Sensor Interface, I2C, Memory Interface
- Memories (SDRAM & Flash)
- Ethernet Phy & Connector
- 3Mpixel Color Image Sensor



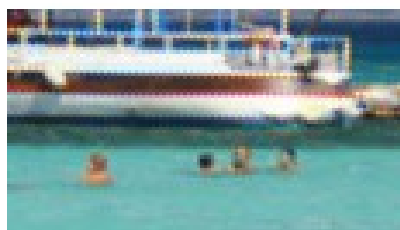
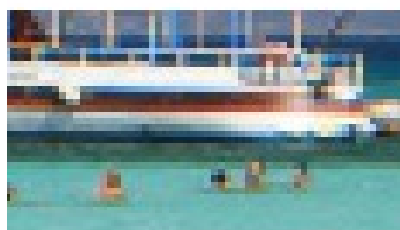
Figure 1: 4to4 simple demosaic



Figure 2: 4to1 simple demosaic



Figure 3: Interpolation (3x3)



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